REMARKS

Examiner J. Maldonado is thanked for the thorough examination and search of the subject Patent Application. Claims 1 and 9 have been amended. Claims 4, 5, 7, 8, 13, 14, 16, 17, 22, and 23 have been canceled.

All Claims are believed to be in condition for Allowance, and that is so requested.

Reconsideration of Claims 1-3 and 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes et al (U.S. 4,536,951) in view of Huang et al (U.S. 6,180,509) and in view of Liu (U.S. 5,693,568) and in view of Wang et al (U.S. 6,080,660 B1) is requested based on Amended Claim 1 and on the following remarks.

Applicant has amended Claim 1 to now include the limitations wherein the etch stop layer comprises a tantalum containing film and wherein the etch stop layer acts as an etch stop during the etching of the second metal layer to form vias. In particular, Amended Claim 1 now reads:

1. (Currently Amended) A method of forming self-aligned, anti-via interconnects in an integrated circuit device comprising:

providing a semiconductor substrate;

depositing a first metal layer overlying said semiconductor substrate;

depositing an etch stop layer overlying said first metal layer wherein said etch stop layer comprises a ~~tungsten~~ tantalum containing film;

depositing a second metal layer overlying said etch stop layer;

depositing an anti-reflective coating layer comprising titanium nitride overlying said second metal layer;

etching through said second metal layer, said etch stop layer, and said first metal layer to form connective lines;

thereafter etching through said second metal layer to form vias wherein said etch stop layer acts as an etch stop;

thereafter depositing a dielectric layer overlying said vias, said connective lines and said semiconductor substrate; and

polishing down said dielectric layer to complete said self-aligned, anti-via interconnects in the manufacture of

the integrated circuit device.

Applicant notes that the cited art of Rhodes et al, Huang et al, Lie et al, and Wang et al do not appear to teach or to suggest an etch stopping layer comprising a tantalum containing film. In addition, Applicant has carefully reviewed Ye et al (U.S. Patent 4,536,951) that has been cited with respect to Claims 9-12, 15, and 18-21 below. Ye et al does describe tantalum nitride barrier layers 214 and 218 that underlie and overlie a conductive copper layer 216 in Figs. 2A-2G. In addition, in Figs. 3A-3G, tantalum nitride barrier layers 314 and 318 underlie and overlie a conductive copper layer 316. Each of these examples differ substantially from the present invention because Ye et al does not teach or suggest a method for using these layers as an etching stop. In particular, in reference to Fig. 2E, Ye et al states:

"FIG. 2E shows the plasma etching stack after transfer of the pattern through tantalum nitride barrier layer 218, copper layer 216, and tantalum nitride barrier layer 214 to the upper surface of silicon dioxide dielectric layer 212. (column 12, lines 63-64)"

Fig. 2E shows the etching step removing all three layers 218, 216, and 214 down to the silicon dioxide 212.

Similarly, with reference to Fig. 3E, Ye et al states:

"FIG. 3E shows the transfer of the pattern through tantalum nitride barrier layer 318, copper layer 316, and tantalum nitride barrier layer 314 to the upper surface of silicon dioxide dielectric layer 312. (column 15, lines 19-22)"

Fig. 3E shows the etching step removing the top two layers 218 and 216 while layer 214 remains. However, this is not consistent with the text. In addition, the text provides no indication that the lower tantalum nitride barrier layer 214 is used in anyway as an etching stop.

Applicant clearly teaches in the Specification, page 12, "that the etch stop layer 62 stops the etching process from attacking the underlying first metal layer 58. In this way, the second metal layer 66 is completely etched through without etching the first metal layer 58." Further, this illustrated in Fig. 6 of the Drawings. Applicant has amended Claim 1 to make clear this distinctive feature of Applicant's claimed invention. Further, Applicant believes that the cited art of Rhodes et al,

Huang et al, Liu, Wang et al, and, importantly, Ye et al do not teach or suggest, separately or taken together, the above-described feature of Applicant's claimed invention such that one skilled in the art at the time of the invention could practice the claimed invention.

In light of the above, Applicant believes that Claim 1 should not be rejected under 35 USC 103(a). Further, Claims 2-3 and 6 represent patentably distinct, further limitations on Claim 1 that should likewise not be rejected under 35 USC 103(a).

Reconsideration of Claims 1-3 and 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes et al (U.S. 4,536,951) in view of Huang et al (U.S. 6,180,509) and in view of Liu (U.S. 5,693,568) and in view of Wang et al (U.S. 6,080,660 B1) is requested based on Amended Claim 1 and on the above remarks.

Reconsideration of Claims 9-12, 15, 18-21 rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes et al (U.S. 4,536,951) in view of Ye et al (U.S. 6,080,529), in view of Huang et al (U.S. 6,180,509) in view of Liu et al (U.S.

5,693,568) and in view of Pangrle et al (U.S. 6,713,382) is requested based on Amended Claim 9 and on the following remarks.

Applicant has amended Claim 9 in similar fashion as Amended Claim 1. In particular, Amended Claim 9 now reads:

9. (Currently Amended) A method of forming self-aligned, anti-via interconnects in an integrated circuit device comprising:

providing a semiconductor substrate;

depositing a first metal layer overlying said semiconductor substrate;

depositing an etch stop layer overlying said first metal layer wherein said etch stop layer comprises a tantalum containing film;

depositing a second metal layer overlying said etch stop layer;

depositing an anti-reflective coating layer comprising titanium nitride overlying said second metal layer;

etching through said second metal layer, said etch stop layer, and said first metal layer to form connective lines;

thereafter etching through said second metal layer to form vias wherein said etch stop layer acts as an etch stop;

thereafter depositing a dielectric layer overlying said vias, said connective lines and said semiconductor substrate wherein said dielectric layer is SiOF (fluorinated silica glass), SiOC (C-substituted siloxane), amorphous SiC:H, MSQ (methylsilsesquioxane), porous materials, PPXC polymer (poly(chloro-p-xylylene), PPXN polymer (poly-p-xylylene), or VT-4 (tetrafluoro-p-xylylene); and

polishing down said dielectric layer to complete said self-aligned, anti-via interconnects in the manufacture of the integrated circuit device wherein said anti-reflective coating layer is a polishing stop.

As discussed above, the cited art of Rhodes et al, Ye et al, Huang et al, Liu et al, do not teach or suggest the limitation added to Claim 9 by amendment. In addition, while Pangrle et al does mention using tantalum nitride as a barrier layer (column 9, lines 30-33), the reference does not teach or suggest using this tantalum nitride as an etching stop for etching through a top metal layer while not etching a lower metal layer as is taught in the claimed invention. Therefore,

Applicant believes that Amended Claim 9 should not be rejected under 35 USC 103(a). Further, Claims 10-12 and 15 represent patentable further limitations on Amended Claim 9 and should not be rejected under 35 U.S.C. 103(a) if Claim 9 is not rejected. In addition, Claim 18 maintains the key limitations of an etching stop comprising a tantalum containing film wherein this film is used as an etching stop for the via metal etch. Therefore, Applicant believes that Claim 18 should not be rejected under 35 USC 103(a). Further, Claims 19-21 represent patentable further limitations on Claim 18 and should not be rejected under 35 U.S.C. 103(a) if Claim 18 is not rejected.

Reconsideration of Claims 9-12, 15, 18-21 rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes et al (U.S. 4,536,951) in view of Ye et al (U.S. 6,080,529), in view of Huang et al (U.S. 6,180,509) in view of Liu et al (U.S. 5,693,568) and in view of Pangrle et al (U.S. 6,713,382) is requested based on Amended Claim 9 and on the above remarks.

Applicants have reviewed the prior art made of record and not relied upon and have discussed their impact on the present invention above.

Allowance of all Claims is requested.

It is requested that should the Examiner not find that the Claims are now Allowable that the Examiner call the undersigned at 989-894-4392 to overcome any problems preventing allowance.

Respectfully submitted,

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